EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week7 Report

3/6/20 - 3/13/20
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member, FPGA focus
Zixuan Guo - Team member, FPGA focus
Justin Sung - Team member, FPGA focus

Weekly Summary

- Have communication with SPI and Core processor on the Nano
- Finished work on schematics for PCB design and start to work on Layout
- Confirm the functionality and accuracy of the Librosa library and other open-source libraries for sound processing
- Develop a full diagram for how the software will be integrated onto hardware devices.
- Port the MAC design into Libero IDE and confirm functionality

Past Week Accomplishments

- MAC Design - Zixuan Guo
    - Start to put the MAC accelerator on the FPGA design and able to read and write to the SRAM on the FPGA.
    - Able to communicate with the SPI and the AMBA protocol.

- PCB Design - Jake Meiss
    - Finished the PCB schematics view and move on to the layout design
    - Updated parts list with current discrete component selections

- SW - Jake Tener
    - Work on extending Python model training script with C++ sound analysis library
    - Design full overarching design diagram for how the software will be integrated onto the embedded system
    - Progress on applying full project application into languages and frameworks that can be accelerated onto hardware.

- HW - Justin Sung, Andrew Vogler

    - Continue progress towards establishing SPI data communications between the MSP430 and the NANO.
    - SPI connection established
    - Generated code for MSP430 as slave device

Pending Issues

- Data transmission is not being caught by the SPI core in the Nano.
- Extending python script with C++ is not working as intended. May need to find work around
- Coronavirus implications on project. We will not be able to attend lab to work on applying software to hardware. Also meeting together and with client will get extremely hard.

Individual Contributions

Team Member	**Contribution**	**Weekly Hours**	**Total Hours**
Jake Tener	SW	16	57
Jake Meiss	PCB Design	19	67
Andrew Vogler	HW	15	57
Zixuan Guo	MAC Design	14	55
Justin Sung	HW	17	60

Plans for Coming Week

- Achieve functional data transfer between SPI and Core processor
    - Be able to write data from NANO to MSP430
    - Be able to transfer data between MAC and the other logic components
- Integrate the MAC design into Libero IDE
- Electrical Design
    - Finish the preliminary schematics and begin to get them checked
    - Start on the layout for the PCB
- Software
    - Finish program to generate coefficients that model with expect that also will be able to be applied to the embedded system
    - Consider beginning to move hardware side of things as we worry more about project integration and communication between devices.